

MIPS reference card

add	rd, rs, rt	Add	$rd = rs + rt$	R 0 / 20	registers						
sub	rd, rs, rt	Subtract	$rd = rs - rt$	R 0 / 22	\$0 \$zero						
addi	rt, rs, imm	Add Imm.	$rt = rs + imm_{\pm}$	I 8	\$1 \$at						
addu	rd, rs, rt	Add Unsigned	$rd = rs + rt$	R 0 / 21	\$2-\$3 \$v0-\$v1						
subu	rd, rs, rt	Subtract Unsigned	$rd = rs - rt$	R 0 / 23	\$4-\$7 \$a0-\$a3						
addiu	rt, rs, imm	Add Imm. Unsigned	$rt = rs + imm_{\pm}$	I 9	\$8-\$15 \$t0-\$t7						
mult	rs, rt	Multiply	$\{hi, lo\} = rs * rt$	R 0 / 18	\$16-\$23 \$s0-\$s7						
div	rs, rt	Divide	$lo = rs / rt; hi = rs \% rt$	R 0 / 1a	\$24-\$25 \$t8-\$t9						
multu	rs, rt	Multiply Unsigned	$\{hi, lo\} = rs * rt$	R 0 / 19	\$26-\$27 \$k0-\$k1						
divu	rs, rt	Divide Unsigned	$lo = rs / rt; hi = rs \% rt$	R 0 / 1b	\$28 \$gp						
mfhi	rd	Move From Hi	$rd = hi$	R 0 / 10	\$29 \$sp						
mflo	rd	Move From Lo	$rd = lo$	R 0 / 12	\$30 \$fp						
and	rd, rs, rt	And	$rd = rs \& rt$	R 0 / 24	\$31 \$ra						
or	rd, rs, rt	Or	$rd = rs rt$	R 0 / 25	hi —						
nor	rd, rs, rt	Nor	$rd = \sim(rs rt)$	R 0 / 27	lo —						
xor	rd, rs, rt	eXclusive Or	$rd = rs \wedge rt$	R 0 / 26	PC —						
andi	rt, rs, imm	And Imm.	$rt = rs \& imm_0$	I c	c0 \$13 c0_cause						
ori	rt, rs, imm	Or Imm.	$rt = rs imm_0$	I d	c0 \$14 c0_epc						
xori	rt, rs, imm	eXclusive Or Imm.	$rt = rs \wedge imm_0$	I e							
sll	rd, rt, sh	Shift Left Logical	$rd = rt \ll sh$	R 0 / 0	syscall codes						
srl	rd, rt, sh	Shift Right Logical	$rd = rt \gg sh$	R 0 / 2	for MARS/SPIM						
sra	rd, rt, sh	Shift Right Arithmetic	$rd = rt \gg sh$	R 0 / 3	1 print integer						
sllv	rd, rt, rs	Shift Left Logical Variable	$rd = rt \ll rs$	R 0 / 4	2 print float						
srlv	rd, rt, rs	Shift Right Logical Variable	$rd = rt \gg rs$	R 0 / 6	3 print double						
srav	rd, rt, rs	Shift Right Arithmetic Variable	$rd = rt \gg rs$	R 0 / 7	4 print string						
slt	rd, rs, rt	Set if Less Than	$rd = rs < rt ? 1 : 0$	R 0 / 2a	5 read integer						
sltu	rd, rs, rt	Set if Less Than Unsigned	$rd = rs < rt ? 1 : 0$	R 0 / 2b	6 read float						
slti	rt, rs, imm	Set if Less Than Imm.	$rt = rs < imm_{\pm} ? 1 : 0$	I a	7 read double						
sltiu	rt, rs, imm	Set if Less Than Imm. Unsigned	$rt = rs < imm_{\pm} ? 1 : 0$	I b	8 read string						
j	addr	Jump	$PC = PC \& 0xF0000000 (addr_0 \ll 2)$	J 2	9 sbrk/alloc. mem.						
jal	addr	Jump And Link	$\$ra = PC + 8; PC = PC \& 0xF0000000 (addr_0 \ll 2)$	J 3	10 exit						
jr	rs	Jump Register	$PC = rs$	R 0 / 8	11 print character						
jalr	rs	Jump And Link Register	$\$ra = PC + 8; PC = rs$	R 0 / 9	12 read character						
beq	rt, rs, imm	Branch if Equal	$if (rs == rt) PC += 4 + (imm_{\pm} \ll 2)$	I 4	13 open file						
bne	rt, rs, imm	Branch if Not Equal	$if (rs != rt) PC += 4 + (imm_{\pm} \ll 2)$	I 5	14 read file						
syscall		System Call	$c0_cause = 8 \ll 2; c0_epc = PC; PC = 0x80000080$	R 0 / c	15 write to file						
lui	rt, imm	Load Upper Imm.	$rt = imm \ll 16$	I f	16 close file						
lb	rt, imm(rs)	Load Byte	$rt = SignExt(M_1[rs + imm_{\pm}])$	I 20	exception causes						
lbu	rt, imm(rs)	Load Byte Unsigned	$rt = M_1[rs + imm_{\pm}] \& 0xFF$	I 24	0 interrupt						
lh	rt, imm(rs)	Load Half	$rt = SignExt(M_2[rs + imm_{\pm}])$	I 21	1 TLB protection						
lhu	rt, imm(rs)	Load Half Unsigned	$rt = M_2[rs + imm_{\pm}] \& 0xFFFF$	I 25	2 TLB miss L/F						
lw	rt, imm(rs)	Load Word	$rt = M_4[rs + imm_{\pm}]$	I 23	3 TLB miss S						
sb	rt, imm(rs)	Store Byte	$M_1[rs + imm_{\pm}] = rt$	I 28	4 bad address L/F						
sh	rt, imm(rs)	Store Half	$M_2[rs + imm_{\pm}] = rt$	I 29	5 bad address S						
sw	rt, imm(rs)	Store Word	$M_4[rs + imm_{\pm}] = rt$	I 2b	6 bus error F						
ll	rt, imm(rs)	Load Linked	$rt = M_4[rs + imm_{\pm}]$	I 30	7 bus error L/S						
sc	rt, imm(rs)	Store Conditional	$M_4[rs + imm_{\pm}] = rt; rt = atomic ? 1 : 0$	I 38	8 syscall						
pseudo-instructions					9 break						
bge	rx, ry, imm	Branch if Greater or Equal	R <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 60px;">op</td><td style="width: 60px;">rs</td><td style="width: 60px;">rt</td><td style="width: 60px;">rd</td><td style="width: 60px;">sh</td><td style="width: 60px;">func</td></tr></table>	op	rs	rt	rd	sh	func		a reserved instr.
op	rs	rt	rd	sh	func						
bgt	rx, ry, imm	Branch if Greater Than				b coproc. unusable					
ble	rx, ry, imm	Branch if Less or Equal	I <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 60px;">op</td><td style="width: 60px;">rs</td><td style="width: 60px;">rt</td><td style="width: 160px;">imm</td></tr></table>	op	rs	rt	imm			c arith. overflow	
op	rs	rt	imm								
blt	rx, ry, imm	Branch if Less Than				F: fetch instr.					
la	rx, label	Load Address	J <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td style="width: 60px;">op</td><td style="width: 200px;">addr</td></tr></table>	op	addr			L: load data			
op	addr										
li	rx, imm	Load Immediate				S: store data					
move	rx, ry	Move register									
nop		No Operation									