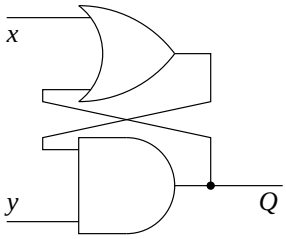
Question 12.2–1: (Solution, p 3)

For the circuit below, fill in the truth table at right to represent how the value of Q changes based on the inputs x and y. Notice that you should ignore two of the rows.

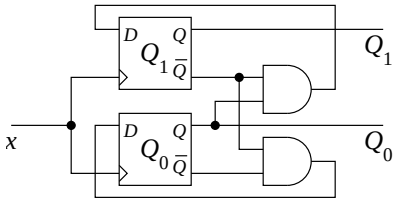


x	y	old Q	new Q
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	(ignore)
1	0	1	(ignore)
1	1	0	
1	1	1	

Question 12.2–2: (Solution, p 3) How is a D flip-flop's behavior different from a D latch's behavior?

Question 12.2–3: (Solution, p 3)

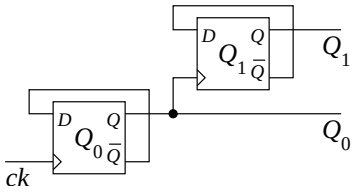
Suppose the upper D flip-flop in the below circuit were holding 1 and the lower D flip-flop held 0, while the x input were 0. At right, tabulate how the circuit's output changes as the input x toggles between 0 and 1.



x	Q_1	Q_0
0	1	0
1		
0		
1		
0		
1		
0		
1		

Question 12.2–4: (Solution, p 3)

Suppose that both of the flip-flops in the below circuit currently hold 0. Tabulate how the circuit at left changes as the input ck toggles through the inputs at left.



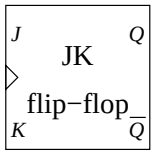
ck	Q_1	Q_0
0		
1		
0		
1		
0		
1		
0		
1		
0		
1		

Question 12.3–1: (Solution, p 3) Draw a circuit with a single input T and a single output, where the output toggles to a different value each time T changes from 0 to 1. (Your circuit may incorporate D flip-flops.) The following table illustrates how your circuit would change.

T	Q	explanation
0	0	
1	1	T changes to 1, so Q changes
0	1	T changes to 0; Q remains at 1
1	0	T changes to 1, so Q changes
0	0	T changes to 0; Q remains at 0
1	1	T changes to 1, so Q changes

Question 12.3–2: (Solution, p 3) Using two D flip-flops, design a circuit that takes a single input ck and outputs two bits $Q_1\,Q_0$, whose values cycle to the next number of the sequence $00, 01, 11, 10, 00, 01, 11, 10, \ldots$ each time ck changes from 0 to 1. (Note that this is not a two-bit counter: 11 comes after 10.)

Question 12.3–3: (Solution, p 4) Recall the JK flip-flop.



transition table

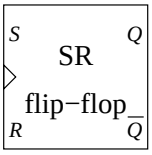
J	K	new Q
0	0	old Q
0	1	0
1	0	1
1	1	$\overline{\text{old } Q}$

activation table

old Q	new Q	J	K
0	0	0	d
0	1	1	d
1	0	d	1
1	1	d	0

Using two JK flip-flops, design a circuit with a single input wire, representing a clock, and a single output wire, which shows 1 on every third clock pulse. Thus, the output should read 0, 0, 1, 0, 0, 1... Show your intermediate work.

Question 12.3–4: (Solution, p 4) Suppose we could had SR flip-flops, defined as follows.



transition table

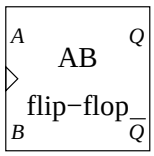
S	R	new Q
0	0	old Q
0	1	0
1	0	1
1	1	avoid

activation table

old Q	new Q	S	R
0	0	0	d
0	1	1	0
1	0	0	1
1	1	d	0

Using two SR flip-flops, design a circuit that takes a single clock input and produces two outputs representing a two-bit binary number. Each clock cycle, the represented output number should go through the next number in the cycle 0, 1, 3, 2, 0, 1, 3, 2, 0.... Show your intermediate work.

Question 12.3–5: (Solution, p 4) Suppose somebody were to define an AB flip-flop.



transition table

A	B	new Q
0	0	0
0	1	old Q
1	0	$\overline{\text{old } Q}$
1	1	1

activation table

old Q	new Q	A	B
0	0	0	d
0	1	1	d
1	0	d	0
1	1	d	1

Using two AB flip-flops, design a circuit with a single input wire, representing a clock, and a two output wires o_1 and o_0, which should progress through the binary numbers 0 through 3 before repeating the sequence (00, 01, 10, 11, 00, 01, 10, 11,...). Show your intermediate work.

Solution 12.2–1: (Question, p 1)

x	y	old Q	new Q
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	(ignore)
1	0	1	(ignore)
1	1	0	1
1	1	1	1

Solution 12.2–2: (Question, p 1) In a D flip-flop, the memory value changes only at that instant that the $clock$ input becomes 1. In a latch, however, the memory value continues adopting any values given as long as its set input is 1. (In other words: In a D flip-flop, if the D input changes while $clock$ remains 1, the remembered value doesn't change. In a latch, however, any change to the D input while set is 1 results in an immediate change to the remembered value.)

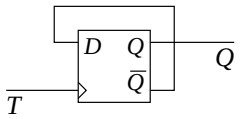
Solution 12.2–3: (Question, p 1)

x	Q_1	Q_0
0	1	0
1	0	0
0	0	0
1	0	1
0	0	1
1	1	0
0	1	0
1	0	0

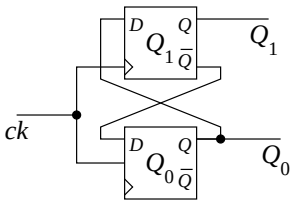
Solution 12.2–4: (Question, p 1)

ck	Q_1	Q_0
0	0	0
1	1	1
0	1	1
1	1	0
0	1	0
1	0	1
0	0	1
1	0	0
0	0	0
1	1	1

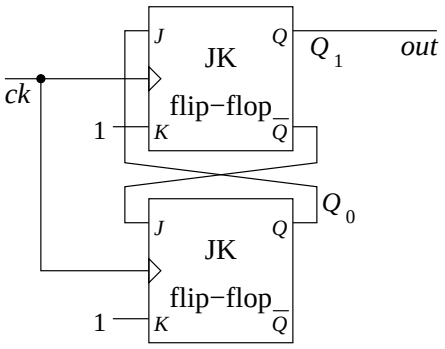
Solution 12.3–1: (Question, p 2)



Solution 12.3–2: (Question, p 2)



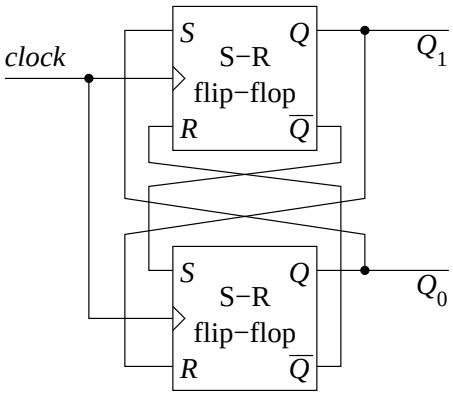
Solution 12.3–3: (Question, p 2)



Work leading up to this solution:

old		new						
Q_1	Q_0	Q_1	Q_0	J_1	K_1	J_0	K_0	out
0	0	0	1	0	d	1	d	0
0	1	1	0	1	d	d	1	0
1	0	0	0	d	1	0	d	1
1	1	d	d	d	d	d	d	d
expressions				Q_0	1	$\overline{Q_1}$	1	Q_1

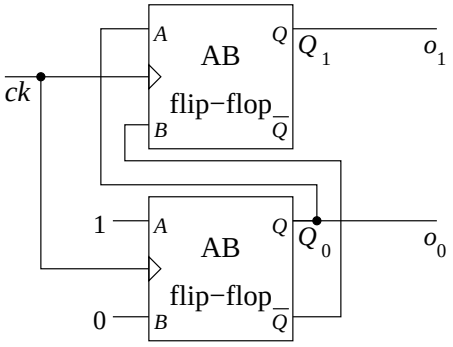
Solution 12.3–4: (Question, p 2)



Work leading up to answer:

old		new					
Q_1	Q_0	Q_1	Q_0	S_1	R_1	S_0	R_0
0	0	0	1	0	d	1	0
0	1	1	1	1	0	d	0
1	0	0	0	0	1	0	d
1	1	1	0	d	0	0	1
expressions				Q_0	$\overline{Q_0}$	$\overline{Q_1}$	Q_1

Solution 12.3–5: (Question, p 2)



Work leading up to answer:

old		new					
Q_1	Q_0	Q_1	Q_0	A_1	B_1	A_0	B_0
0	0	0	1	0	d	1	d
0	1	1	0	1	d	d	0
1	0	1	1	d	1	1	d
1	1	0	0	d	0	d	0
expressions				Q_0	$\overline{Q_0}$	1	0